REMARKS

Claims 2 - 16, 18 - 20, 27, 28, 30 - 44, and 58 - 73 will be the only pending claims under consideration upon entry of this amendment.

Claim 57 is cancelled herein.

Claims 58 - 73 have been added herein.

Claim 2 has been amended herein to include all of the limitations of cancelled independent claim 57, from which claim 2 directly depended prior to the present amendment, and to delete "tantalum silicide, and niobium silicide" from the group of silicides.

Claims 2, 58 and 65 are independent.

Rejection of claims 57, 2, 3, 6, 8, 15, 35, 36 and 40 under 35 U.S.C. §103(a)

Claims 57, 2, 3, 6, 8, 15, 35, 36 and 40 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Cutter et al. (US 6,323,536) in view of Mayer et al. (Electronic Materials Science: For Integrated Circuits in Si and GaAs, pp. 294-295).

The applicant has cancelled claim 57.

The Examiner rejected claim 2, which (prior to the present amendment) depended directly from claim 57, citing that "Cutter et al. further disclose that the silicide (642) is a refractory metal silicide (col. 8, line 1), which can be niobium silicide or tantalum silicide."

As shown above, the applicant has amended claim 2 by adding all of the limitations of cancelled independent claim 57, making claim 2 an independent claim. In addition, claim 2 has been amended to remove niobium silicide and tantalum silicide from the group of claimed silicides. It is respectfully submitted that claim 2 is patentable, because the silicides recited in

claim 2, namely cobalt silicide, platinum silicide, nickel silicide, chromium silicide, and palladium silicide, are not anticipated or rendered obvious by Cutter, which discloses only refractory metal silicides.

The Examiner rejected claim 3, stating that "Cutter et al. further disclose that the antifuse layer (610) may comprise silicon dioxide (col. 8, lines 17-1 9)."

Claim 3 depends directly from patentable claim 2, and Applicant submits that claim 3 is patentable for at least this reason.

The Examiner rejected claim 6, stating that "Cutter et al. further disclose for the semiconductor device of claim 2 that the conductive layer or semiconductor layer (614) on and in contact with the antifuse layer (610) may be a metal layer (col. 8, lines 27-28)."

Claim 6 depends directly from patentable claim 2, and Applicant submits that claim 6 is patentable for at least this reason.

The Examiner rejected claim 8, stating that "Cutter et al. further comprise a first silicon layer (640) (col. 8, line 2), the silicide layer (642) on and in contact with the first silicon layer (640)."

Claim 8 depends from patentable claims 6 and 2, and Applicant submits that claim 8 is patentable for at least this reason.

The Examiner rejected claim 15, stating that "Cutter et al, further disclose for the semiconductor device of claim 6 that the conductive layer (614) comprises a metal (col. 8, lines 27-28)."

Claim 15 depends from patentable claims 6 and 2, and Applicant submits that claim 15 is patentable for at least this reason.

The Examiner rejected claim 35, stating:

> Cutter et al. in view of Mayer et al. disclose the semiconductor device of claim 2.
>
> Cutter et al, in view of Mayer et al. differ from the claimed invention by not showing that the grown dielectric antifuse layer was grown by oxidizing or nitriding the silicide.
>
> Mayer et al. disclose oxidation of silicides (10.7 Oxidation of Silicides and Fig. 10.19) to grow dielectric SiO_2 on a silicide layer (lines 5-7 of 10.7 Oxidation of Silicides).
>
> Since both Cutter et al. and Mayer et al. teach a method of fabricating a semiconductor device comprising a silicide layer, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. in view of Mayer et al. with the dielectric SiO_2 layer grown by oxidizing the silicide disclosed by Mayer et al., because the combined semiconductor device would have a dielectric SiO_2 layer with less contamination and thus of better quality due to the fact that the SiO_2 can be grown right after silicide formation.

Claim 35 depends directly from patentable claim 2, and Applicant submits that claim 35 is patentable for at least this reason.

The Examiner rejected claim 36, stating:

> Cutter et al. in view of Mayer et al. disclose the semiconductor device of claim 2.
>
> Cutter et at. further disclose that the silicide lay Page 5 contact with the polysilicon layer (640) (col. 8, line 2 and Fig. 6B).
>
> Cutter et al. in view of Mayer et al. differ from the claimed invention by not showing that the polysilicon layer in contact with the silicide layer is lightly doped or intrinsic, and therefore the electrical connection between the silicide layer and the conductive layer or semiconductor layer is an electrical connection between a Schottky diode and a conductor.
>
> Cutter et al. further disclose that the bottom conductor (112) (col. 1, line 21) of a semiconductor device (Fig. 1) comprising an antifuse layer (110)

(col. 1, line 20) is in contact with n- region (126), forming a Schottky diode.

Since Cutter et al. teach a method of fabricating a semiconductor device comprising an antifuse layer, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al, in view of Mayer et al. with the Schottky diode structure disclosed by Cutter et al. to make a semiconductor device comprising a Schottky diode formed between the silicide layer as a bottom conductor and the semiconductor n- region at the bottom and a conductor at the top, because the combined semiconductor device would form a diode device after programming the antifuse layer.

Claim 36 depends directly from patentable claim 2, and Applicant submits that claim 36 is patentable for at least this reason.

The Examiner rejected claim 40, stating that "Cutter et al. further disclose that the silicide (642) is a portion of the Schottky diode (640 and 642 combined)."

Claim 40 depends indirectly from patentable claim 2, and Applicant submits that claim 40 is patentable for at least this reason.

Rejection of claims 4 and 5 under 35 U.S.C. §103(a)

Claims 4 and 5 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Cutter et al. (US 6,323,536) in view of Mayer et al. (Electronic Materials Science: For Integrated Circuits in Si and GaAs, pp. 294-295) as applied to claim 2 above, and further in view of Arghavani et al. (US 5,780,346).

The Examiner rejected claim 4 stating:

Cutter et al. in view of Mayer et al. disclose the semiconductor device of claim 2.

Cutter et al. further disclose that the dielectric antifuse layer (61 0) may comprise a combination of layers (col. 8, lines 21-22), which can

be silicon dioxide and silicon nitride (col. 8, lines 17-1 9).

Cutter et al. in view of Mayer et al. differ from the claimed invention by not showing that the grown dielectric antifuse layer comprises nitrogen.

Arghavani et al. disclose a semiconductor device (Fig. 3K) where silicon oxynitride (365 and 366) (col. 6, lines 15 and 16) is formed by nitridation of silicon oxide (360) (col. 5, lines 66 - col. 6, line 2).

Since both Cutter et al. and Arghavani et al, teach a semiconductor device, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. in view of Mayer et al. with the oxynitride layer disclosed by Arghavani et al. to have the grown dielectric antifuse layer comprise nitrogen, because the combined semiconductor device would prevent dopant outdiffusion from the silicide layer or polysilicon layer when polysilicon is used as a semiconductor layer on and in contact with the antifuse layer.

Claim 4 depends directly from patentable claim 2, and Applicant submits that claim 4 is patentable for at least this reason.

The Examiner rejected claim 5, stating:

Cutter et al. in view of Mayer et al. and further in view of Arghavani et al. disclose the semiconductor device of claim 4.

Cutter et al. in view of Mayer et al. and further in view of Arghavani et al. differ from the claimed invention by not showing that the grown dielectric antifuse layer comprises silicon nitride or silicon oxynitride.

Arghavani et al. disclose a semiconductor device (Fig. 3K) where silicon oxynitride (365 and 366) (col. 6, lines 15 and 16) is formed by nitridation of silicon oxide (360) (col. 5, lines 66 - col. 6, line 2).

Since both Cutter et al. and Arghavani et al. teach a semiconductor device, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. in view of Mayer et al. and further in view of Arghavani

> et al, with the oxynitride layer grown by nitridation of silicon dioxide disclosed by Arghavani et al., because the combined semiconductor device would prevent dopant outdiffusion from the silicide layer or polysilicon layer when polysilicon is used as a semiconductor layer on and in contact with the antifuse layer.

Claim 5 depends from patentable claims 4 and 2, and Applicant submits that claim 5 is patentable for at least this reason.

Rejection of claim 7 under 35 U.S.C. §103(a)

Claim 7 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Cutter et al. (US 6,323,536) in view of Mayer et al. (Electronic Materials Science: For Integrated Circuits in Si and GaAs, pp. 294-295) as applied to claim 6 above, and further in view of Chen (US 200310062594).

The Examiner rejected claim 7 stating:

> Cutter et al. in view of Mayer et al. differ from the claimed invention by not showing that the grown dielectric antifuse layer is less than about 50 angstroms thick.
>
> Chen discloses a semiconductor device (Fig. 11) comprising a dielectric antifuse layer (60) (line 3 of [0027]) where the bottom oxide layer (57) (line 5 of [0027]) in the dielectric antifuse layer (60) is less than about 50 angstroms thick (lines 7-9 of [0027]).
>
> Since both Cutter et al. and Chen teach a semiconductor device comprising a dielectric antifuse layer, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. in view of Mayer et al. with the thickness of the silicon dioxide disclosed by Chen, because the combined semiconductor device would be programmed at an intended low voltage by causing dielectric breakdown, while controlling leakage between the silicide layer and the conductive layer.

Applicant submits that the Examiner has misapplied Chen to Claim 7. As stated by the Examiner, Chen discloses a dielectric

antifuse layer (60) (line 3 of [0027]). Dielectric antifuse layer (60) is composed of three layers: bottom oxide layer 57, a silicon nitride layer 58 and a top oxide layer 59. Layer 57 has a thickness of 10 - 50 angstroms, layer 58 has a thickness of 45 angstroms, and layer 59 has a thickness of 40 - 80 angstroms. (lines 7- 22 of [0027]) Thus, the dielectric antifuse layer disclosed in Chen has a minimum thickness of 10 + 45 + 40 = 95 angstroms. Claim 7 is limited to a dielectric antifuse which is less than about 50 angstroms thick and is therefore not anticipated by or obvious in light of the cited references. Applicant submits that for this reason, in addition to claim 7 being dependent on patentable claims 6 and 2, claim 7 is patentable.

Rejection of claims 9 - 11 and 41 under 35 U.S.C. §103(a)

Claims 9 - 11 and 41 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Cutter et al. (US 6,323,536) in view of Mayer et al. (Electronic Materials Science: For Integrated Circuits in Si and GaAs, pp. 294-295) as applied to claim 2 above, and further in view of Choi (US 5,242,851).

The Examiner rejected claim 9, stating:

> In regards to claim 9, Cutter et al. in view of Mayer et al. disclose the semiconductor device of claim 2.
>
> Cutter et al. further disclose that the top conductor (614) may comprise polysilicon (col. 8, lines 27-28).
>
> Cutter et al. in view of Mayer et al. differ from the claimed invention by not showing that the conductor or semiconductor layer on and in contact with the grown dielectric antifuse layer is a lightly doped or intrinsic semiconductor layer.
>
> Choi discloses a programmable interconnect device (Fig. 3P) comprising a dielectric antifuse layer (14) (col. 6, lines 6-7) and an intrinsic polysilicon layer (16) (col. 6, line 11) deposited on the dielectric antifuse layer (14).

> Since both Cutter et al, and Choi teach a semiconductor memory comprising a dielectric antifuse layer, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. in view of Mayer et al. with the intrinsic semiconductor layer disclosed by Choi, because the combined semiconductor device would reduce off-state leakage due to the combination of the silicide layer as a bottom electrode and the intrinsic semiconductor layer as a top electrode. (emphasis added)

Applicant submits that the Examiner has misapplied Choi to claim 9. Claim 9 contains the limitation "wherein the conductor or semiconductor layer on and in contact with the grown dielectric antifuse layer is a lightly doped or intrinsic semiconductor layer." (emphasis added). It is clear that the "conductor or semiconductor layer" is not a dielectric layer which breaks down, but rather is a top conducting layer. The examiner interprets the intrinsic polysilicon layer (16)(col. 6, line 11) of Choi as a top electrode (see above). To the contrary, however, the intrinsic polysilicon layer of Choi is a dielectric layer which breaks down upon application of a sufficient voltage. Referring to Fig. 1A,

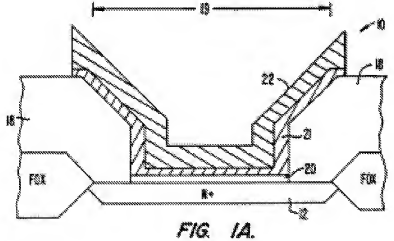

FIG. 1A.

Choi states:

> Silicon dioxide 18 is etched to form a contact opening 19. A dielectric antifuse layer includes first and second layers 21 and 22 overlying the part lower conductive layer 12 exposed by the contact opening 19. (Col 2, line 65 - 68) . . . In contact opening 19, a relatively thin first layer of silicon dioxide 20 is formed on conductive layer 12. The first silicon dioxide 20 has a thickness in the range of 50 to 120 Angstroms. A second layer of intrinsic polycrystalline silicon (poly) 21 in the range of 100 to 3000 Angstroms covers the top surface of the first silicon dioxide layer 20 and is extended onto the top surface of insulating layer 18. On the top surface of the first intrinsic poly layer 21, an upper conductive layer 22 is deposited and is extended onto the top surface of insulating layer 18. Suitable materials for the upper conductive layer 22 include aluminum and alloys of aluminum, molybdenum, and tungsten.
>
> In the unprogrammed state the second intrinsic poly layer 21 acts as a very high resistance barrier between conductive layers 22 and 12. In the programmed state the first [*sic*] intrinsic poly layer 21 undergoes a transition from a very high resistance path to a very low resistance conductive path. (emphasis added)

Thus, intrinsic polysilicon layer 21 of Choi (which corresponds to the intrinsic polysilicon layer 16 cited by the Examiner in relation to Fig. 3P) is itself an antifuse layer and not a conductor or electrode layer as interpreted by the Examiner.

The cited references therefore do not teach the use of a lightly doped or intrinsic semiconductor layer as a top conductor or semiconductor layer as required by claim 9, and Applicant submits that claim 9 is patentable for this reason as well as because claim 9 depends directly from patentable claim 2.

The Examiner rejected claim 10, stating:

> Cutter et al. in view of Mayer et al. and further in view of Choi disclose the semiconductor device of claim 9.

> Cutter et al. in view of Mayer et al. and further in view of Choi differ from the claimed invention by not showing that the intrinsic semiconductor layer forms a portion of a Schottky diode.
>
> Choi discloses a programmable interconnect device (Fig. 3P) further comprising an aluminum layer (20) (col. 6, line 49) deposited on the intrinsic polysilicon layer (16), forming a Schottky diode.
>
> Since both Cutter et al. and Choi teach a semiconductor memory comprising a dielectric antifuse layer, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al, in view of Mayer et al. and further in view of Choi with the Schottky diode structure disclosed, by Choi, because the combined semiconductor device would form a diode device after programming the antifuse layer.

Claim 10 depends from patentable claims 9 and 2, and Applicant submits that claim 10 is patentable for at least this reason.

The Examiner rejected claim 11, stating:

> Cutter et al. in view of Mayer et al. and further in view of Choi disclose the semiconductor device of claim 10.
>
> Cutter et al. in view of Mayer et al. and further in view of Choi differ from the claimed invention by not showing that the intrinsic semiconductor layer forms a portion of a Schottky diode after breakdown of the grown dielectric antifuse layer.
>
> It is inherent that the intrinsic semiconductor layer disclosed by Choi to form a portion of a Schottky diode after breakdown of the grown dielectric antifuse layer, because the intrinsic semiconductor layer will be brought in contact with the silicide layer after breakdown of the grown dielectric antifuse layer.

Claim 11 depends from patentable claims 10, 9 and 2, and Applicant submits that claim 10 is patentable for at least this reason.

The Examiner rejected claim 41, stating:

In regards to claim 41, Cutter et al. in view of Mayer et al. disclose the semiconductor device of claim 2.

Cutter et al. further disclose that the silicide layer (642) is in contact with the polysilicon layer (640) (col. 8, line 2) (Fig. 6B).

Cutter et al. in view of Mayer et al. differ from the claimed invention by not showing that the electrical connection between the silicide layer and the conductive layer or semiconductor layer is an electrical connection between portions of a Schottky diode.

Cutter et al. further disclose that the bottom conductor (112) (col. 1, line 21) of a semiconductor device (Fig. 1) comprising an antifuse layer (110) (col. 1, line 20) is in contact with n-region (126), forming a Schottky diode.

Since Cutter et al. teach a method of fabricating a semiconductor device comprising an antifuse layer, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. in view of Mayer et al. with the Schottky diode structure disclosed by Cutter et al. to make a semiconductor device comprising a Schottky diode formed between the silicide layer as a bottom conductor and the semiconductor n- region, because the combined semiconductor device would form a diode device after programming the antifuse layer.

Further regarding claim 41, Cutter et al. in view of Mayer et al. differ from the claimed invention by not showing that the conductive layer or semiconductor layer is a portion of a Schottky diode, and therefore the electrical connection between the silicide layer and the conductive layer or semiconductor layer is an electrical connection between portions of a Schottky diode.

Choi discloses a programmable interconnect device (Fig. 3P) comprising a dielectric antifuse layer (14) (col. 6, lines 6-7), an intrinsic polysilicon layer (16) (col. 6, lines 11) deposited on the dielectric antifuse layer (14), and an aluminum layer (20) (col. 6, line 49) deposited on the intrinsic polysilicon layer (16), forming a Schottky diode.

Since both Cutter et al. and Choi teach a semiconductor memory comprising an antifuse layer, it would have been obvious to the one of ordinary skill

in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. in view of Mayer et al. comprising a Schottky diode between the silicide layer and the bottom semiconductor layer with the Schottky diode formed between the intrinsic semiconductor layer and the top conductor layer disclosed by Choi, because the combined semiconductor device would form a diode device comprising two Schottky diodes in series after programming the antifuse layer.

Applicant submits that it is not proper to combine Cutter et al. in view of Mayer et al. with Choi, and, even if it were proper, the combination does not disclose the use of an antifuse layer between the portions of a Schottky diode.

The combination of Cutter et al. in view of Mayer et al. with Choi is improper. The antifuse layer of Choi is an intrinsic polysilicon layer alone or in combination with an oxide layer (col. 6 lines 65 - 68). This intrinsic polysilicon antifuse layer cannot be grown on a silicide as required by Cutter et al. in view of Mayer et al., and by claim 41. Therefore, the combination of references is improper.

In addition, the Examiner bases the propriety of the combination on "the Schottky diode formed between the intrinsic semiconductor layer and the top conductor layer disclosed by Choi". The Choi structure cited by the Examiner does not form a Schottky diode. First, before sufficient voltage is applied across the intrinsic semiconductor layer (16) in Fig. 3P and (21) in Fig. 1, the intrinsic semiconductor layer acts as an insulator and no current flows in either direction through the structure. Thus, the pre-programming structure is not a diode. Once sufficient voltage is applied across the structure, the intrinsic semiconductor layer breaks down, the intrinsic semiconductor layer becomes a conductor layer, and is no longer a semiconductor. See Choi Col. 3 lines 14 - 27. Thus, the post-

programming structure is not a diode either. The Examiner's rationale for combining the references is faulty.

Even if the combination were proper, the combination would not provide the structural limitations of claim 41, i.e., "wherein the electrical connection between the silicide layer and the conductive layer or semiconductor layer is an electrical connection between portions of a Schottky diode." If the Choi antifuse structure of metal layer (20) (col. 6 line 49) lying atop the intrinsic polysilicon (16) (col. 6 lines 10 - 13) were inserted into the semiconductor structure of Cutter et al. in view of Mayer et al. the structure from top to bottom would be metal layer/intrinsic polysilicon antifuse layer/(optional oxide layer)/silicide layer. After the antifuse layer is broken down, the functional structure would be metal conductor/broken down antifuse conductor/silicide conductor. Thus, the broken down antifuse would not form an electrical connection between portions of a Schottky diode, but rather between two conductors.

For the foregoing reasons, and because claim 41 depends directly from patentable claim 2, Applicant submits that claim 41 is patentable over the cited references.

Rejection of claims 12 - 14 under 35 U.S.C. §103(a)

Claims 12 - 14 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Cutter et al. (US 6,323,536) in view of Mayer et al. (Electronic Materials Science: For Integrated Circuits in Si and GaAs, pp. 294-295) and further in view of Choi (US 5,242,851) as applied to claim 11 above, and further in view of Van Brocklin et al. (US 6,703,652).

The Examiner rejected claim 12, stating:

> Cutter et al. in view of Mayer et al, and further in view of Choi disclose the semiconductor device of claim 11.

Cutter et al. in view of Mayer et al. and further in view of Choi differ from the claimed invention by not showing that the Schottky diode is a portion of a memory cell.

Van Brocklin et al. disclose a memory cell (Fig. 1A and Fig. 1 B) (col. 2, lines 28- 29) where an antifuse is a voltage breakdown element (106) (col. 2, lines 38-39).

Since both Cutter et al. and Van Brocklin et al. teach a method of fabricating a semiconductor memory, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. in view of Mayer et al. and further in view of Choi with the memory cell disclosed by Van Brocklin et al. to make a semiconductor device comprising an antifuse layer including a Schottky diode, because the combined semiconductor device would form a diode device after programming the antifuse layer.

Claim 12 depends from patentable claims 11, 9 and 2, and Applicant submits that claim 12 is patentable for at least this reason.

The Examiner rejected claim 13, stating:

Cutter et al. in view of Mayer et al, and further in view of Choi and then further in view of Van Brocklin et al. disclose the semiconductor device of claim 12.

Cutter et al. in view of Mayer et al. and further in view of Choi and then further in view of Van Brocklin et al. differ from the claimed invention by not showing that the memory cell is a portion of a memory array.

Van Brocklin et al. further disclose that the memory cell (Fig. 1A and Fig. 1 B) is a portion of a memory array (Fig. 2A and Fig. 2B) (col. 3, lines 40-43).

Since both Cutter et al. and Van Brocklin et al. teach a method of fabricating a semiconductor memory, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. in view of Mayer et al. and further in view of Choi and then further in view of Van Brocklin et al. with the memory array disclosed by Van Brocklin et

al., because the combined semiconductor device could be used in a high density semiconductor memory.

Claim 13 depends from patentable claims 12, 11, 9 and 2, and Applicant submits that claim 13 is patentable for at least this reason.

The Examiner rejected claim 14, stating:

> Cutter et al. in view of Mayer et al. and further in view of Choi and then further in view of Van Brocklin et al. disclose the semiconductor device of claim 13.
>
> Cutter et al. in view of Mayer et al. and further in view of Choi and then further in view of Van Brocklin et al. differ from the claimed invention by not showing that the memory array is a monolithic three dimensional memory array.
>
> Van Brocklin et al. further disclose that the memory array (Fig. 2A and Fig. 2B) is a monolithic three dimensional memory array (Fig. 2C) (col. 3, lines 63-65).
>
> Since both Cutter et al. and Van Brocklin et al, teach a method of fabricating a semiconductor memory, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. in view of Mayer et al. and further in view of Choi and then further in view of Van Brocklin et al. with the three dimensional memory array disclosed by Van Brocklin et al., because the combined semiconductor device could be used in a high density semiconductor memory.

Claim 14 depends from patentable claims 13, 12, 11, 9 and 2, and Applicant submits that claim 14 is patentable for at least this reason.

Rejection of claim 16 under 35 U.S.C. §103(a)

Claim 16 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Cutter et al. (US 6,323,536) in view of Mayer et al. (Electronic Materials Science: For Integrated Circuits in Si and GaAs, pp. 294-295) as applied to claim 15 above, and further in view of Cleeves et at. (US 6,541,312).

The Examiner rejected claim 16, stating:

> Cutter et al. in view of Mayer et al. disclose the semiconductor device of claim 15.
>
> Cutter et al. in view of Mayer et al. differ from the claimed invention by not showing that the conductive layer forms a portion of a Schottky diode.
>
> Cleeves et al. disclose an antifuse stack structure (Fig. 14F) where a lightly doped semiconductor layer (P-) is deposited on a conductor layer (CONDUCTOR), forming a Schottky diode.
>
> Since both Cutter et al. and Cleeves et al. teach a semiconductor device comprising an antifuse layer, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. in view of Mayer et al. with the Schottky diode structure disclosed by Cleeves et al., because the combined semiconductor device would form a diode device after programming the dielectric antifuse layer.

Claim 16 depends from patentable claims 15, 6 and 2, and Applicant contends that claim 16 is patentable for at least this reason.

Rejection of claims 18 - 20 under 35 U.S.C. §103(a)

Claims 18 - 20 were rejected under 35 U.S.C. §103(a) as being unpatentable over Cutter et al. (US 6,323,536) in view of Mayer et al. (Electronic Materials Science: For Integrated Circuits in Si and GaAs, pp. 294-295) and further in view of Cleeves et al. (US 6,541,312) as applied to claim 16 above, and further in view of Van Brocklin et al. (US 6,703,652).

The Examiner rejected claim 18, stating:

Cutter et al. in view of Mayer et al. and further in view of Cleeves et al. disclose the semiconductor device of claim 16.

Cutter et al. in view of Mayer et al. and further in view of Cleeves et al. differ from the claimed invention by not showing that the Schottky diode is a portion of a memory cell.

Van Brocklin et al. disclose a memory cell (Fig. 1A and Fig. 1 B) (col. 2, lines 28- 29) where an antifuse is a voltage breakdown element (1 06) (col. 2, lines 38-39).

Since both Cutter et al. and Van Brocklin et al. teach a method of fabricating a semiconductor memory, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. in view of Mayer et al. and further in view of Cleeves et al. with the memory cell disclosed by Van Brocklin et al. to make a semiconductor device comprising an antifuse layer including a Schottky diode, because the combined semiconductor device would form a diode device after programming the antifuse layer.

Claim 18 depends from patentable claims 16, 15, 6 and 2, and Applicant submits that claim 18 is patentable for at least this reason.

The examiner rejected claim 19, stating:

Cutter et al. in view of Mayer et al. and further in view of Cleeves et al. and then further in view of Van Brocklin et al. disclose the semiconductor device of claim 18.

Cutter et al. in view of Mayer et al. and further in view of Cleeves et al. and then further in view of Van Brocklin et al. differ from the claimed invention by not showing that the memory cell is a portion of a memory array.

Van Brocklin et al. further disclose that the memory cell (Fig. 1A and Fig. 1 B) is a portion of a memory array (Fig. 2A and Fig. 2B) (col. 3, lines 40-43).

Since both Cutter et al. and Van Brocklin et al, teach a method of fabricating a semiconductor memory, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter

et al. in view of Mayer et al, and further in view of Cleeves et al. and then further in view of Van Brocklin et al. with the memory array disclosed by Van Brocklin et al., because the combined semiconductor device could be used in a high density semiconductor memory.

Claim 19 depends from patentable claims 18, 16, 15, 6 and 2, and Applicant submits that claim 19 is patentable for at least this reason.

The Examiner rejected claim 20, stating:

> Cutter et al. in view of Mayer et al. and further in view of Cleeves et al. and then further in view of Van Brocklin et al. disclose the semiconductor device of claim 19.
>
> Cutter et al. in view of Mayer et al, and further in view of Cleeves et al. and then further in view of Van Brocklin et al. differ from the claimed invention by not showing that the memory array is a monolithic three dimensional memory array.
>
> Van Brocklin et al. further disclose that the memory array (Fig. 2A and Fig. 28) is a monolithic three dimensional memory array (Fig. 2C) (col. 3, lines 63-65).
>
> Since both Cutter et al. and Van Brocklin et al. teach a method of fabricating a semiconductor memory, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. in view of Mayer et al. and further in view of Cleeves et al. and then further in view of Van Brocklin et al. with the three dimensional memory array disclosed by Van Brocklin et al., because the combined semiconductor device could be used in a high density semiconductor memory.

Claim 20 depends from patentable claims 19, 18, 16, 15, 6 and 2, and Applicant submits that claim 20 is patentable for at least this reason.

Rejection of claims 27, 33 and 34 under 35 U.S.C. §103(a)

Claims 27, 33 and 34 were rejected uncer 35 U.S.C. §103(a) as being unpatentable over Cutter et al. (US 6,323,536) in view

of Mayer et al. (Electronic Materials Science: For Integrated Circuits in Si and GaAs, pp. 294-295) as applied to claim 6 above, and further in view of Hart et al. (US 5,726,484).

The Examiner rejected claim 27, stating:

> Cutter et al. in view of Mayer et al, disclose the semiconductor device of claim 6.
>
> Cutter et al. in view of Mayer et al. differ from the claimed invention by not showing that the conductive layer comprises titanium nitride.
>
> Hart et al. disclose a semiconductor device comprising an antifuse (Fig. 1A) where titanium nitride-layer (101) (col. 5, lines 40-44) is deposited on the antifuse layer (105) (col. 5, line 31).
>
> Since both Cutter et al. and Hart et al. disclose a semiconductor device comprising an antifuse layer, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. in view of Mayer et al. with the titanium nitride conductive layer disclosed by Hart et al., because the combined semiconductor device could use titanium nitride against diffusion of copper atoms when copper is used as interconnect material.

Claim 27 depends from patentable claims 6 and 2, and Applicant submits that claim 27 is patentable for at least this reason.

The Examiner rejected claim 33 stating:

> Cutter et al. in view of Mayer et al, and further in view of Hart et al. disclose the semiconductor device of claim 27.
>
> Cutter et al. in view of Mayer et al. and further in view of Hart et al. differ from the claimed invention by not showing that for a portion of the conductive layer more than about 20 angstroms thick, the density of the titanium nitride is less than about 4.0 grams per cubic cm.
>
> The claim is prima facie obvious without showing that the claimed ranges achieve unexpected results relative to the prior art range. In re Woodruff, 16 USPQ2d 1935, 1937 (Fed. Cir. 1990). See also In re Huang, 40 USPQ2d 1685, 1688 (Fed. Cir. 1.996) (claimed ranges of a result effective variable, which do not overlap the prior art ranges, are unpatentable unless

they produce a new and unexpected result which is different in kind and not merely in degree from the results of the prior art). See also In re Boesch, 205 USPQ 215 (CCPA) (discovery of optimum value of result effective variable in known process is ordinarily within skill of art) and In re Aller, 105 USPQ 233 (CCPA 1955) (selection of optimum ranges within prior art general conditions is obvious).

Claim 33 depends from patentable claims 27, 6 and 2, and Applicant submits that claim 33 is patentable for at least this reason.

The Examiner rejected claim 34, stating:

> Cutter et al. in view of Mayer et al. and further in view of Hart et al. disclose the semiconductor device of claim 27.
>
> Cutter et al. in view of Mayer et al, and further in view of Hart et al. differ from the claimed invention by not showing that for a portion of the film more than about 20 angstroms thick, the resistivity of the titanium nitride is greater than about 300 microOhms-cms.
>
> The claim is prima facie obvious without showing that the claimed ranges achieve unexpected results relative to the prior art range. In re Woodruff, 16 USPQ2d 1935, 1937 (Fed. Cir. 1990). See also In re Huang, 40 USPQ2d 1685, 1688 (Fed. Cir. 1996) (claimed ranges of a result effective variable, which do not overlap the prior art ranges, are unpatentable unless they produce a new and unexpected result which is different in kind and not merely in degree from the results of the prior art). See also In re Boesch, 205 USPQ 21 5 (CCPA) (discovery of optimum value of result effective variable in known process is ordinarily within skill of art) and In re Aller, 105 USPQ 233 (CCPA 1955) (selection of optimum ranges within prior art general conditions is obvious).

Claim 34 depends from patentable claims 27, 6 and 2, and Applicant submits that claim 34 is patentable for at least this reason.

Rejection of claim 28 under 35 U.S.C. §103(a)

Claim 28 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Cutter et al. (US 6,323,536) in view of Mayer et al. (Electronic Materials Science: For Integrated Circuits in Si and GaAs, pp. 294-295) and further in view of Hart et al. (US 5,726,484) as applied to claim 27 above, and further in view of Cleeves et al. (US 6,541,312).

The examiner rejected claim 28, stating:

> Cutter et al. in view of Mayer et al. and further in view of Hart et al. disclose the semiconductor of claim 27.
>
> Cutter et al. in view of Mayer et al. and further in view of Hart et al. differ from the claimed invention by not showing that the conductive layer forms a portion of a Schottky diode.
>
> Cleeves et al. disclose an antifuse stack structure (Fig. 14F) where a lightly doped semiconductor layer (P-) is deposited on a conductor layer (CONDUCTOR), forming a Schottky diode. Since both Cutter et al. and Cleeves et al. teach a semiconductor device comprising an antifuse layer, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. in view of Mayer et al, and further in view of Hart et al. with the Schottky diode structure disclosed by Cleeves et al., because the combined semiconductor device would form a diode device after programming the dielectric antifuse layer.

Claim 28 depends from patentable claims 27, 6 and 2, and Applicant submits that claim 28 is patentable for at least this reason.

Rejection of claims 30 - 32 under 35 U.S.C. §103(a)

Claims 30 - 32 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Cutter et al. (US 6,323,536) in view of Mayer et al. (Electronic Materials Science: For Integrated Circuits in Si and GaAs, pp. 294-295) and further in view of

Hart et al. (US 5,726,484) and then further in view of Cleeves et al. (US 6,541,312) as applied to claim 28 above, and further in view of Van Brocklin et al. (US 6,703,652). The teachings of Cutter et al. in view of Mayer et al. and further in view of Hart et al. and then further in view of Cleeves et al. are discussed above.

The examiner rejected claim 30, stating:

> Cutter et al. in view of Mayer et al. and further in view of Hart et al. and then further in view of Cleeves et al. disclose the semiconductor device of claim 28.
>
> Cutter et al. in view of Mayer et al. and further in view of Hart et al. and then further in view of Cleeves et al. differ from the claimed invention by not showing that the Schottky diode is a portion of a memory cell.
>
> Van Brocklin et al. disclose a memory cell (Fig. 1A and Fig. 1 B) (col. 2, lines 28- 29) where an antifuse is a voltage breakdown element (106) (col. 2, lines 38-39).
>
> Since both Cutter et al. and Van Brocklin et al. teach a method of fabricating a semiconductor memory, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. in view of Mayer et al. and further in view of Hart et al. and then further in view of Cleeves et al. with the memory cell disclosed by Van Brocklin et al. to make a semiconductor device comprising an antifuse layer, a titanium nitride conductive layer and a Schottky diode, because the combined semiconductor device would form a diode device after programming the antifuse layer.

Claim 30 depends from patentable claims 28, 27, 6 and 2, and Applicant submits that claim 30 is patentable for at least this reason.

The Examiner rejected claim 31, stating

> Cutter et al. in view of Mayer et al. and further in view of Hart et al. and then further in view of Cleeves et al, and then further in view of Van

Brocklin et al. disclose the semiconductor device of claim 30.

Cutter et al. in view of Mayer et al. and further in view of Hart et al. and then further in view of Cleeves et al. and then further in view of Van Brocklin et al. differ from the claimed invention by not showing that the memory cell is a portion of a memory array.

Van Brocklin et al. further disclose that the memory cell (Fig. 1A and Fig. 1 B) is a portion of a memory array (Fig. 2A and Fig. 2B) (col. 3, lines 40-43).

Since both Cutter et al. and Van Brocklin et al. teach a method of fabricating a semiconductor memory, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. in view of Mayer et al, and further in view of Hart et al, and then further in view of Cleeves et al. and then further in view of Van Brocklin et al. with the memory array disclosed by Van Brocklin et al., because the combined semiconductor device could be used in a high density semiconductor memory.

Claim 31 depends from patentable claims 30, 28, 27, 6 and 2, and Applicant submits that claim 31 is patentable for at least this reason.

The Examiner rejected claim 32, stating:

Cutter et al. in view of Mayer et al, and further in view of Hart et al. and then further in view of Cleeves et al, and then further in view of Van Brocklin et al. disclose the semiconductor device of claim 31.

Cutter et al. in view of Mayer et al, and further in view of Hart et al. and then further in view of Cleeves et al, and then further in view of Van Brocklin et al. differ from the claimed invention by not showing that the memory array is a monolithic three dimensional memory array.

Van Brocklin et al. further disclose that the memory array (Fig. 2A and Fig. 2B) is a monolithic three dimensional memory array (Fig. 2C) (col. 3, lines 63-65).

Since both Cutter et al. and Van Brocklin et al. teach a method of fabricating a semiconductor memory, it would have been obvious to the one of ordinary

skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. in view of Mayer et al. and further in view of Hart et al. and then further in view of Cleeves et al. and then further in view of Van Brocklin et al. with the three dimensional memory array disclosed by Van Brocklin et al., because the combined semiconductor device could be used in a high density semiconductor memory.

Claim 32 depends from patentable claims 31, 30, 28, 27, 6 and 2, and Applicant submits that claim 32 is patentable for at least this reason.

Rejection of claims 37 - 39 under 35 U.S.C. §103(a)

Claims 37 - 39 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Cutter et al. (US 6,323,536) in view of Mayer et al. (Electronic Materials Science: For Integrated Circuits in Si and GaAs, pp. 294-295) as applied to claim 36 above, and further in view of Van Brocklin et al. (US 6,703,652). The teachings of Cutter et al. in view of Mayer et al, are discussed above.

The examiner rejected claim 37 stating:

> Cutter et al. in view of Mayer et al. disclose the semiconductor device of claim 36.
>
> Cutter et al. in view of Mayer et al. differ from the claimed invention by not showing that the Schottky diode is a portion of a memory cell.
>
> Van Brocklin et al. disclose a memory cell (Fig. 1A and Fig. 1B) (col. 2, lines 28- 29) where an antifuse is a voltage breakdown element (106) (col. 2, lines 38-39).
>
> Since both Cutter et al. and Van Brocklin et al. teach a method of fabricating a semiconductor memory, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. in view of Mayer et al. with the memory cell disclosed by Van Brocklin et al. to make a semiconductor device comprising an antifuse layer including a Schottky diode, because the combined

semiconductor device would form a diode device after programming the antifuse layer.

Claim 37 depends from patentable claims 36 and 2, and Applicant submits that claim 37 is patentable for at least this reason.

The Examiner rejected claim 38, stating:

> Cutter et al. in view of Mayer et al, and further in view of Van Brocklin et al. disclose the semiconductor device of claim 37.
>
> Cutter et al. in view of Mayer et al. and further in view of Brocklin et al. differ from the claimed invention by not showing that the memory cell is a portion of a memory array.
>
> Van Brocklin et al. further disclose that the memory cell (Fig. 1A and Fig. 1B) is a portion of a memory array (Fig. 2A and Fig. 2B) (col. 3, lines 40-43).
>
> Since both Cutter et al. and Van Brocklin et al, teach a method of fabricating a semiconductor memory, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. in view of Mayer et al. and further in view, of Van Brocklin et al. with the memory array disclosed by Van Brocklin et al., because the combined semiconductor device could be used in a high density semiconductor memory.

Claim 38 depends from patentable claims 37, 36 and 2, and Applicant submits that claim 38 is patentable for at least this reason.

The Examiner rejected claim 39, stating:

> Cutter et al. in view of Mayer et al. and further in view of Van Brocklin et al. disclose the semiconductor device of claim 38.
>
> Cutter et al. in view of Mayer et al. and further in view of Brocklin et al. differ from the claimed invention by not showing that the memory array is a monolithic three dimensional memory array.
>
> Van Brocklin et al. further disclose that the memory array (Fig. 2A and Fig. 2B) is a monolithic three dimensional memory array.(Fig. 2C) (col. 3, lines 63-65).

> Since both Cutter et al. and Van Brocklin et al. teach a method of fabricating a semiconductor memory, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. in view of Mayer et al. and further in view of Van Brocklin et al. with the three dimensional memory array disclosed by Van Brocklin et al., because the combined semiconductor device could be used in a high density semiconductor memory.

Claim 39 depends from patentable claims 38, 37, 36 and 2, and Applicant submits that claim 39 is patentable for at least this reason.

Rejection of claims 42 - 44 under 35 U.S.C. §103(a)

Claims 42 - 44 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Cutter et al. (US 6,323,536) in view of Mayer et al. (Electronic Materials Science: For Integrated Circuits in Si and GaAs, pp. 294-295) and further in view of Choi (US 5,242,851) as applied to claim 41 above, and further in view of Van Brocklin et al. (US 6,703,652).

The Examiner rejected claim 42, stating:

> Cutter et al. in view of Mayer et al. and further in view of Choi disclose the semiconductor device of claim 41.
>
> Cutter et al. in view of Mayer et al. and further in view of Choi differ from the claimed invention by not showing that the Schottky diode is a portion of a memory cell.
>
> Van Brocklin et al. disclose a memory cell (Fig. 1A and Fig. 1 B) (col. 2, lines 28- 29) where an antifuse is a voltage breakdown element (106) (col. 2, lines 38-39).
>
> Since both Cutter et al. and Van Brocklin et al. teach a method of fabricating a semiconductor memory, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. in view of Mayer et al. and further in view of Choi with the memory cell disclosed by Van Brocklin et al., because the combined semiconductor device would

form a diode device comprising a series of Schottky diodes after programming the antifuse layer.

Claim 42 depends from patentable claims 41 and 2, and Applicant submits that claim 42 is patentable for at least this reason.

The Examiner rejected claim 43, stating:

> Cutter et al. in view of Mayer et al, and further in view of Choi and then further in view of Van Brocklin et al. disclose the semiconductor device of claim 42.
>
> Cutter et al. in view of Mayer et al. and further in view of Choi and then further in view of Van Brocklin et al. differ from the claimed invention by not showing that the memory cell is a portion of a memory array.
>
> Van Brocklin et al. further disclose that the memory cell (Fig. 1A and Fig. 1B) is a portion of a memory array (Fig. 2A and Fig. 28) (col. 3, lines 40-43). Since both Cutter et al. and Van Brocklin et al. teach a method of fabricating a semiconductor memory, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. in view of Mayer et al. and further in view of Choi and then further in view of Van Brocklin et al. with the memory array disclosed by Van Brocklin et al., because the combined semiconductor device could be used in a high density semiconductor memory.

Claim 43 depends from patentable claims 42, 41 and 2, and Applicant submits that claim 43 is patentable for at least this reason.

The Examiner rejected claim 44, stating:

> Cutter et al. in view of Mayer et al. and further in view of Choi and then further in view of Van Brocklin et al. disclose the semiconductor device of claim 43.
>
> Cutter et al. in view of Mayer et al. and further in view of Choi and then further in view of Van Brocklin et al. differ from the claimed invention by not showing that the memory array is a monolithic three dimensional memory array.

> Van Brocklin et al. further disclose that the memory array (Fig. 2A and Fig. 2B) is a monolithic three dimensional memory array (Fig. 2C) (col. 3, lines 63-65).
>
> Since both Cutter et al. and Van Brocklin et al. teach a method of fabricating a semiconductor memory, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. in view of Mayer et al. and further in view of Choi and then further in view of Van Brocklin et al. with the three dimensional memory array disclosed by Van Brocklin et al., because the combined semiconductor device could be used in a high density semiconductor memory.

Claim 44 depends from patentable claims 43, 42, 41 and 2, and Applicant submits that claim 44 is patentable for at least this reason.

Rejection of claims 57, 2, 3, 9 and 11 - 14 on ground of non-statutory obviousness-type double patenting

The Applicant will address this rejection upon the allowance of any of the claims rejected thereby.

Addition of claims 58 - 73

Applicant has added new claims 58 - 75.

Independent claim 58 contains the limitations of cancelled claim 57 and the limitations of claim 9. Applicant submits that claim 58 is patentable for the same reasons set forth above with regard to claim 9, with the following exception: Claim 58 does not contain the limitations of claim 2, and so does not share this basis of patentability with claim 9.

Claims 59 - 64 depend directly or indirectly from claim 58, and Applicant submits that they are patentable for at least that reason.

Independent claim 65 contains the limitations of cancelled claim 57 and the limitations of claim 41. Applicant submits that claim 65 is patentable for the same reasons set forth above with regard to claim 41, with the following exception: Claim 65 does not contain the limitations of claim 2, and so does not share this basis of patentability with claim 41.

Claims 66 - 73 depend directly or indirectly from claim 65, and Applicant submits that they are patentable for at least that reason.

CONCLUSION

Applicants believe the claims are now in condition for allowance, and respectfully request reconsideration and allowance of the same.

A separate Request for Extension of Time is enclosed herewith, with authorization to charge the requisite extension fee to Deposit Account No. 04-1696. Applicants do not believe any other Request for Extension of Time is required but if it is, please accept this paragraph as a Request for Extension of Time and authorization to charge the requisite extension fee to Deposit Account No. 04-1696. Applicants do not believe any additional fees are due regarding this Amendment. However, if any additional fees are required, please charge Deposit Account No. 04-1696. The Applicants encourage the Examiner to telephone Applicants' attorney should any questions remain.

Respectfully Submitted,

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Tarrytown, New York